REMARKS

The Examiner rejected claims 1 – 10 under 35 U.S.C. 103(a) as being unpatentable over the prior art disclosed by applicant as shown in Figure 2 of Applicant's application in view of U.S. Patent No. 6,169.435 to Fujii *et al.* In that regard, the Examiner stated:

> "The prior art differs from the claimed invention in that the prior art does not specifically disclose that the second latch-decision circuit receiving the recovered clock signal. However, it is well known to provide clock recovery signal to plurality of latch circuits. In Fig. 1, Fujii et al is cited to show such well known concept. Fujii et al [sic] show recovered clock signal (CLK2) [sic] receives by latch circuits (13a- 13n)."
>
> Claim 1 requires:
>
> "c) a first latch-decision circuit, the first latch-decision circuit receiving the recovered clock signal;
>
> d) a first latch, the first latch coupled to the first latch-decision circuit, the first latch operable to receive the first input data signal; . . .
>
> f) a second latch-decision circuit, the second latch-decision circuit receiving the recovered clock signal;
>
> g) a second latch, the second latch coupled to the second latch-decision circuit."

Thus, Claim 1 expressly requires two latch-decision circuits and two latches. The latch-decision circuits, not the latches, receive a recovered clock signal. The claimed latch-decision circuits are not latches. (The latches are separately claimed elements.) The meaning of the phrase "latch-decision circuit" is expressly defined in the Applicants' specification:

> "The latch-decision circuit 125 is operable to determine, using algorithms known in the art, an appropriate time to latch the input data signal 115 so that the input data signal 115 is sampled near the center portion of each pulse that corresponds to either logic '1' or logic '0.' Such a determination is based upon the timing information that is received from the clock-recovery circuit 120 and information extracted from the input data signal 115." Specification, p. 2, ln. 23 – p. 3, ln. 4.

Thus, a latch-decision circuit is a circuit that is configured to determine **when** to sample an input data signal that is **input** into a latch. The determination is based upon (i) timing information

received from a recovered clock and (ii) information extracted from the input data signal to be sampled.

If the Examiner desires that the above definition be included in Claim 1, the Examiner is hereby authorized to file an Examiner's Amendment that amends Claim 1 to include the following limitation:

> "wherein the first latch-decision circuit is configured to determine when to command the first latch to sample the first input data signal based upon (i) timing information received from the clock-recovery circuit and (ii) information extracted from the first input data signal."

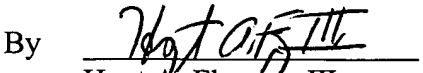
It is improper for the Examiner to ignore the express limitation that two latch-decision circuits, not latches, receive the recovered clock signal when construing the scope of claim 1.

Because Fujii *et al.* does not disclose a latch-decision circuit, much less a plurality of latch-decision circuits that receive a recovered clock signal, claim 1 together with dependent claims 2 – 10, each of which depend from claim 1, are allowable over the art of record.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 
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